REMARKS

The claims remaining in the present application are Claims 1-15. Claim 15 has been added. A proposed amendment to the drawings has been filed herewith in a submission of proposed drawing amendments to correct a minor informality. No new matter has been added as a result of these amendments.

35 U.S.C. §102

Claims 1 – 14 are separately rejected under 35 U.S.C. §102(b) as being anticipated by de Nicolas et al., U.S. Patent No. 5,167,023 (hereinafter, de Nicolas), Goettelmann et al., U.S. Patent No. 5,313,614 (hereinafter, Goettelmann) and Fogg, Jr. et al., U.S. Patent No. 4,951,195 (hereinafter, Fogg). All of the rejections are respectfully traversed.

Claims 1 and 8

Claim 1 recites:

> In a computer which translates instructions from a target instruction set to a host instruction set, a method for determining validity of a translation of a target instruction linked to an earlier translation comprising the steps of:
>
> testing a memory address of a target instruction to be executed against a copy of the memory address of the target instruction from which a translation of the target instruction was made,
>
> executing the translation if the addresses compare, and
>
> generating an exception if addresses do not compare.

Claim 1 recites a method for determining validity of a translation of a target instruction linked to an earlier translation. It is respectfully submitted that de

Nicolas, Goettelmann, and Fogg all fail to disclose determining validity of a translation of a target instruction linked to an earlier translation.

Moreover, Claim 1 recites that the memory address of the target instruction is tested against a copy of the memory address of the target instruction from which a translation of the target instruction was made. It is respectfully submitted that de Nicolas, Goettelmann, and Fogg all fail to disclose this limitation of Claim 1.

For the foregoing rationale, it is respectfully submitted that Claim 1 is not anticipated by de Nicolas, Goettelmann, or Fogg. As such, allowance of Claim 1 is respectfully submitted. Claim 8 recites similar limitations. As such, allowance of Claim 8 is respectfully submitted.

Claims 2 and 9

Claim 2 recites:

> A method as claimed in Claim 1 in which the step of testing a memory address of a target instruction to be executed against a copy of the memory address of the target instruction from which a translation of the target instruction was made is a process separate from the translation of the target instruction.

In Claim 2, the testing of the memory address is a process separate from the translation of the target instruction. For example, when it is not known when the translation is made whether it will be linked to another translation or not, then the prologue process is generated as a separate short prologue when the linking of the two translations occurs. At this time, the preceding translation is provided a jump instruction to the prologue process; and the prologue

completes (if the test is met) with another jump instruction to the succeeding translation.

De Nicolas, Goettelmann, and Fogg all fail to disclose testing a memory address of a target instruction to be executed as a part of a process that is separate from the translation of the target instruction. For support, the rejection cites de Nicolas at col. 5, lines 59-63, and col. 6, lines 1-7. The cited passages disclose a way to reduce the number of host instructions per simulated instructions for the case when an instruction stores to memory. In particular, the passages disclose that when an instruction updates memory, a determination is made as to whether the update is to a video buffer or to a subsequent instruction. However, Applicants do not understand the cited passage to disclose the testing of a memory address of a target instruction to be executed as a part of a process that is separate from the translation of the target instruction. Moreover, Applicants do not understand de Nicolas to disclose the limitations of Claim 2 elsewhere.

With respect to Goettelmann, the rejection cites col. 9, lines 58-62. Applicants do not understand this passage to disclose the claimed limitation. The cited passage reads, "System simulation 57 thereupon carries out the requested service by accessing target machine address space 55 either directly of via target machine system software 58." Applicants do not understand Goettelmann to disclose the testing of a memory address of a target instruction to be executed in this passage. Moreover, Applicants do not understand Goettelmann to disclose the limitations of Claim 2 elsewhere.

With respect to Fogg, the rejection cites col. 11, lines 45-55. Applicants do not understand this passage to disclose the claimed limitation. The first sentence of the cited passage states that translations are saved such that they may be re-used if the processor transfers control to the same address again. However, nothing is disclosed here regarding the testing of a memory address of a target instruction to be executed as a part of a process that is separate from the translation of the target instruction, as claimed. The cited passage goes on to disclose how the next instruction pointer (IP) is determined for instructions that do not transfer control. However, again there is no disclosure as to any testing of a memory address of a target instruction to be executed, as claimed. Moreover, Applicants do not understand Fogg to disclose the limitations of Claim 2 elsewhere.

For the foregoing rationale, it is respectfully submitted that Claim 2 is not anticipated by de Nicolas, Goettelmann, or Fogg. As such, allowance of Claim 2 is respectfully submitted. Claim 9 recites similar limitations. As such, allowance of Claim 9 is respectfully submitted.

Claims 3 and 10

Claim 3 recites:

> A method as claimed in Claim 1 in which the step of testing a memory address of a target instruction to be executed against a copy of the memory address of the target instruction from which a translation of the target instruction was made is included as a part of the translation of the target instruction.

Claim 3 recites that the testing of the memory address is included as a part of the translation of the target instruction. For example, if it is known that the translation will be linked to a previous translation when it is translated and a check of the physical address is required, then the prologue process (described and illustrated in Figure 3) may be included in the translation. In such as case, the preceding translation merely jumps to the next translation where the address consistency process of the prologue is executed before the translation is executed.

De Nicolas, Goettelmann, and Fogg all fail to disclose testing the memory address as a part of the translation of the target instruction. In support of this rejection, the rejection cites de Nicolas at col. 6, lines 1-5. Applicants do not understand this passage to disclose the claimed limitation. Rather, the passage relates to determining whether an instruction is modifying a subsequent instruction or performing a video buffer update. Moreover, Applicants do not understand de Nicolas to disclose the limitations of Claim 3 elsewhere.

With respect to Goettelmann, the rejection cites col. 20, lines 62-66. Applicants do not understand this passage to disclose the claimed limitation. Rather, the passage relates to a mapping process, which is described as substituting, for each disassembled instruction, an equivalent sequence of operations—including side effects—expressed in terms of machine-independent intermediate language (col. 19, lines 3-7). The mapping is disclosed as consisting of adding to the already created intermediate language

code 1) code for fetching operands, 2) the appropriate skeleton, 3) code for storing the result of the instruction, if necessary. Applicants do not understand this passage to disclose testing the memory address as a part of the translation of the target instruction, as claimed. Moreover, Applicants do not understand Goettelmann to disclose the limitations of Claim 3 elsewhere.

With respect to Fogg, the rejection cites col. 16, lines 22-34. Applicants do not understand this passage to disclose the claimed limitation. Rather, the passage relates to a method of addressing memory. For example, after previously describing how an address is generated, the final sentence of the cited passage describes how the address is used to access the memory of the second processing system. However, this passage fails to disclose that testing of the memory address is included as a part of the translation of the target instruction. Referring to col. 15, lines 56-61, Fogg discloses that the translated code is stored in area 157. However, Fogg does not disclose testing of the memory address included as a part of the translation of the target instruction in the passage. Moreover, Applicants do not understand Fogg to disclose the limitations of Claim 3 elsewhere.

For the foregoing rationale, it is respectfully submitted that Claim 3 is not anticipated by de Nicolas, Goettelmann, or Fogg. As such, allowance of Claim 3 is respectfully submitted. Claim 10 recites similar limitations. As such, allowance of Claim 10 is respectfully submitted.

Claims 4 and 11

Claim 4 recites:

> A method as claimed in Claim 1 which includes an additional step of copying a memory address of a target instruction when a translation of the target instruction is made and linked to an earlier translation.

Claim 4 recites that the memory address of a target address is copied when a translation of the target instruction is made and linked to an earlier translation,

De Nicolas, Goettelmann, and Fogg all fail to disclose copying a memory address of a target instruction when a translation of the target instruction is made and linked to an earlier translation. For support, the rejection cites de Nicolas at col. 12, lines 19-25. Applicants do not understand this passage to disclose the claimed limitation. In contrast, de Nicolas discloses at this passage that the data structure in Figure 6 is used to map first processor instruction addresses, which consist of a code segment, to the address in memory of a second processor, where a sequence of second processor instructions performs the same function (col. 12, lines 19-25). However, there is no disclosure that copying is done when a translation of the target instruction is made and linked to an earlier translation, as claimed.

With respect to Goettelmann, the rejection cites col. 30, lines 6-12. Applicants do not understand this passage to disclose the claimed limitation. Rather, the passage relates to binding a translated application to the translated system software and target machine system software (col. 29, lines 66-68). For example, a linking and loading process is described (col. 30, lines 5-16). Applicants do not understand this to be the claimed limitation of copying a

memory address of a target instruction when a translation of the target instruction is made and linked to an earlier translation.

With respect to Fogg, the rejection cites col. 12, lines 15-21, which mirrors de Nicolas at col. 12, lines 19-25. As discussed above, Applicants do not understand this passage to disclose the claimed limitation. For the rationale discussed above for this passage, it is respectfully submitted that Fogg fails to disclose the claimed limitation.

For the foregoing rationale, it is respectfully submitted that Claim 4 is not anticipated by de Nicolas, Goettelmann, or Fogg. As such, allowance of Claim 4 is respectfully submitted. Claim 11 recites similar limitations. As such, allowance of Claim 11 is respectfully submitted.

Claims 5-7 and 12-14 depend from Claim 1 and 8, which are respectfully believed to be allowable. As such, allowance of Claims 5-7 and 12-14 is earnestly submitted.

Claim 15

Claim 15 has been added. It is respectfully submitted that Claim 15 presents allowable subject matter. As such, allowance of Claim 15 is respectfully submitted.

CONCLUSION

In light of the above listed amendment and remarks, reconsideration of the rejected Claims is requested. Based on the arguments and amendment presented above, it is respectfully submitted that Claims 1-15 overcome the rejections of record and, therefore, allowance of Claims 1-15 is earnestly solicited.

Should the Examiner have a question regarding the instant response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,
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